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ComparativeAnalysisOfCMOSTechnology andQCA

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Abstract :*Moore'slawstatesthat,thenumberoftransistorspersquareinchonintegratedcircuitshaddoubledeveryyearandthisisduetothescalingofComplementaryMetalOxideSemiconductortransistorswhichhasdriventheimmensegrowthofthesemiconductorindustryforlastfourdees.Currently,industriesareworkingwith5nmtechnologybutfurtherscaling of transistors leadsto notonlyphysical andtechnologychallenges butalsomaterialandeconomicalchallenges.QuantumCellularAutomata(QCA)beingadvancedtechnologymayprovideawayforincreasedcomputationalcapabilitiesbeyondCMOSlimits.HencewearecomparingCMOScircuitsandQCAstructureswiththehelpofCadenceVirtuosotoolandQCAProsoftware.Inthispaper,wearecomparingboththetechnologiesonthebasis oftheircertainparameters.*

Keywords –*CMOS, QCA, Cadence VIRTUOSO TOOL, QCADesigner, QCAPRO TOOL*

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.

I. INTRODUCTION

QuantumCellularAutomata(QCA)carriesoutaresearchostudyasanalternativetoCMOSVLSI.Simplelogicalcircuits anddesignsuchasANDgate,Inverter,Adderalongwith1BitMemoryCellhavebeenstudiedandlittleworkhasbeen performedoncreatingtheabovecircuitsanddeterminingtheirparameterslikepowerdissipation,delay,andpolarizationandobtainingthewaveforms.ForCMOSVLSItheCADENCVIRTUOSOTOOLisusedtocreateschematics,symbol,the layoutoftheANDgate,NOTgate,Adderand1BitMemoryCell.UsingCadenceVIRTUOSOToolwecanalsoobtain waveformsforTransientanalysis,DCanalysis,ACanalysisetc.ForQuantumCellularAutomatatheQCADesigneris usedfordesigningthegatesandforobtainingtheoutputwaveformsandtheQCAPROTOOLisusedfordetermining thepolarizationandpowerdissipation.

A.QCACell

Itisananostructurewithfourquantumdots.Dotsareplacedwherethechargecansit.Maximumtwoelectrons canfitintothecellbyrepellingeachothertoobtainstableconfigurationwhichrepresentsLogic0(polarization-1)or Logic1(polarization+1).InQCACellElectronscantunnethroughquantumdots.Itisassumedthatthecellwillhavesix dotsatthetimeofimplementationbutonlyfourcornersareshowninQCAcell.Therearedifferentshapesofquantumdot andvariesdependingontheprocess.

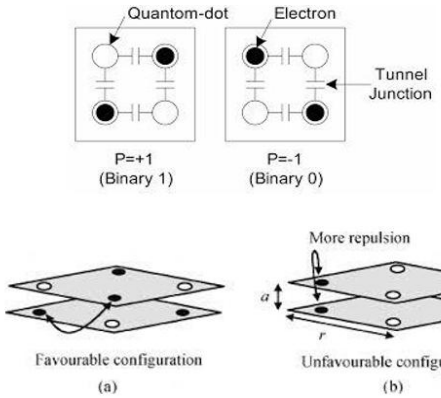

Fig.1.QCACellRepresentation

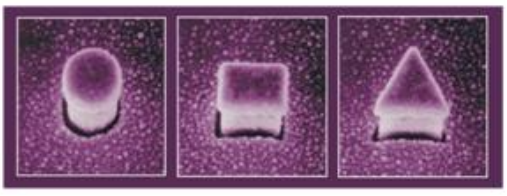

Fig.2.DifferentShapesofQCADots.

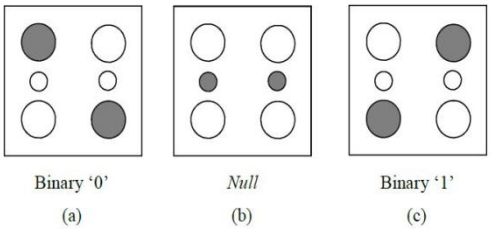

Fig.3.QCACellwith6Dots.

B.QCAWire

Itisanarrangementofquantumdotcellsinseries.InQCAwire,neighboringcellstendtoalignthesamestate.Th us nextcellfollowsthesamelogicleveloftheprevious cell.Inthisway,thedatatransmissiontakesplaceviaQCAwire. UsingCellswhichareorientedat45degreesand90degreeswecanconstructaQCAwire.Awireisdividedintodifferent clockzonessothatsignaldoes notdeteriorateassignaltendsto degradewithalongchainofcellsinthesameclockingzone.

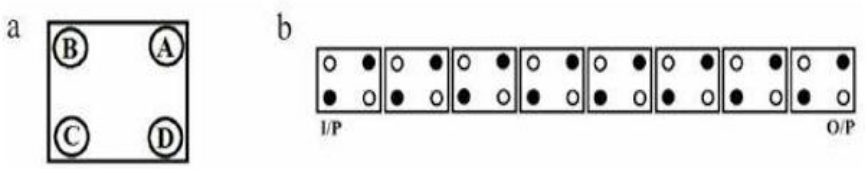

Fig.4.QCAWire.

C.CellClocking

AclockedQCAcircuithassix-dotcellanditrepresentsnull,binary0andbinary1dependingonthepositionofelectrons. Thecellisinanactivestatewhenelectronsareinfourcornerswhileacellisinnullstateorinpolarizationstatewhen cellsareinmiddledots.Ineveryclockscheme,QCAcellfollowsallfourclockphasesswitch,hold,release,relax.In Switchphase,tunnelingbarrierrisesslowlysothatelectronsgetintocornerdots.InHoldphase,tunnelingbarrierremains highandthereforepolarityofthecellalsoremainssame.InReleasephasetunnelingbarrierisreducedslowlythatpulls theelectronsbackintothemiddledots.InRelaxphaseall electronsremaininmiddledotsandthereisnopolarityin cells.

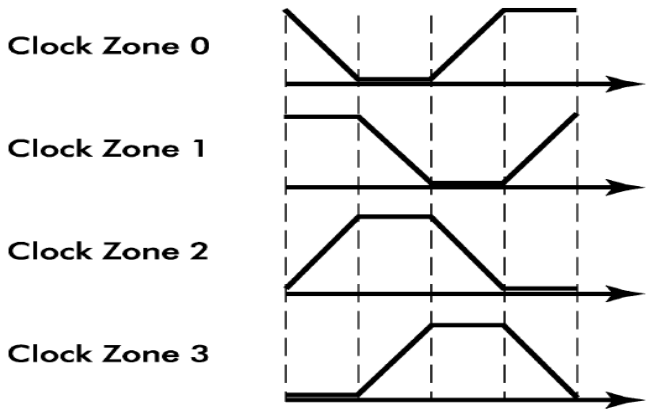

Fig.5.ThefourphasesoftheQCAclock.

II. IMPLEMENTATIONOFCIRCUITS

A.Inverter

Ininverterinputisgivenatoneendandinvertedoutput isobtainedattheend.TheSchematicoftheinverterbased onCMOSissimulatedusingCadenceVirtuosoToolandthe parametersareevaluatedusingacalculatorfunction.Inorder tofindtheareaofthecircuit,wehavetocreatealayout.Area ofthecircuitcanbevariablebasedonplacingandrouting skillsoftheindividual.Thestandarddesignofinverterin QCA isasshownintheFig.6.

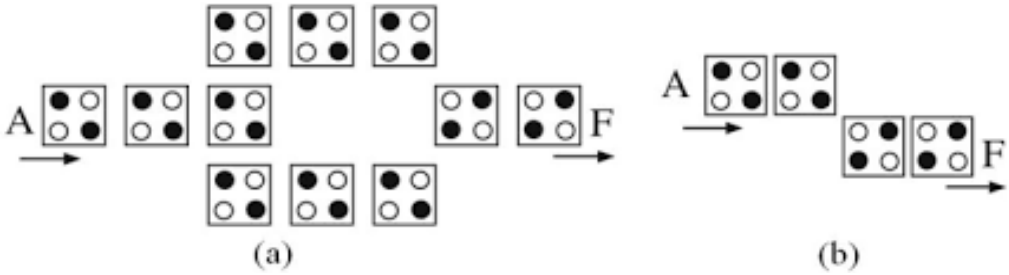

Fig.6.QCAInverterLayout.

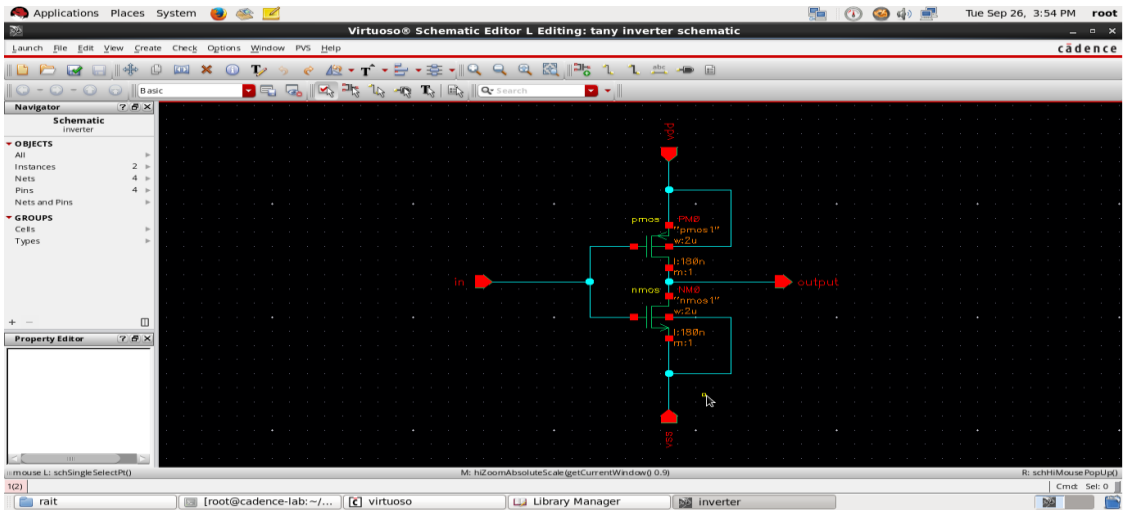

Fig.7.CMOSInverterSchematics.

B.ANDGate

Itisabasicgatewhichimplementslogicalconjunction.IQCAmajoritygateisabasicgateandusingmajoritygate we candesignANDgate.Inmajoritygate,wegettheoutputasamajorityofinputlogic.SofordesigningANDgate,weset afixedpolarizationof-1foroneofthethreeinputs.

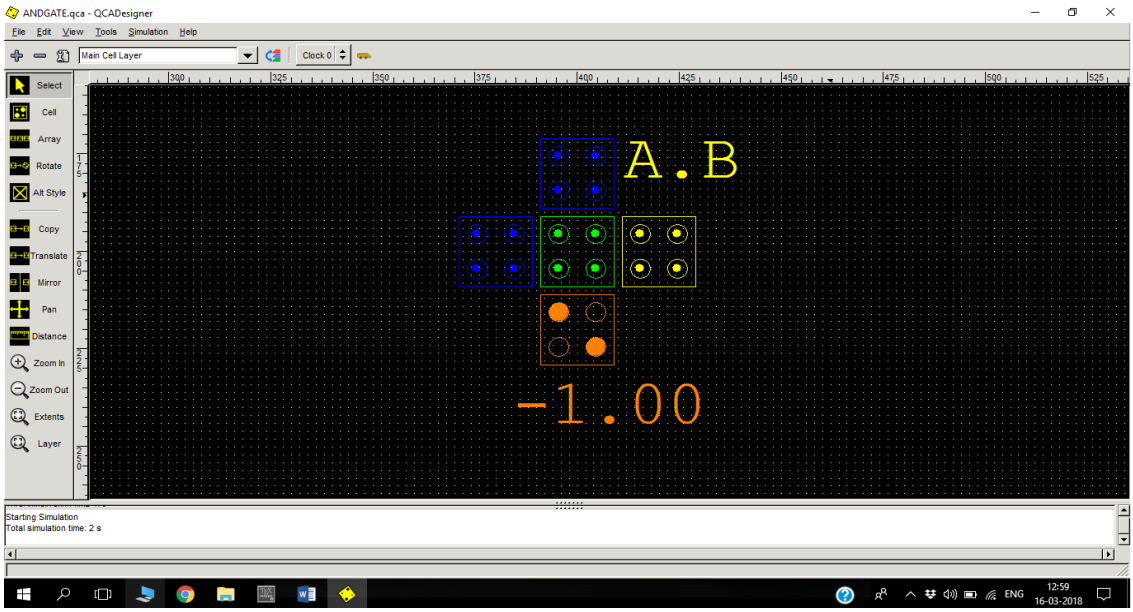

Fig.8.QCAANDGateLayout.

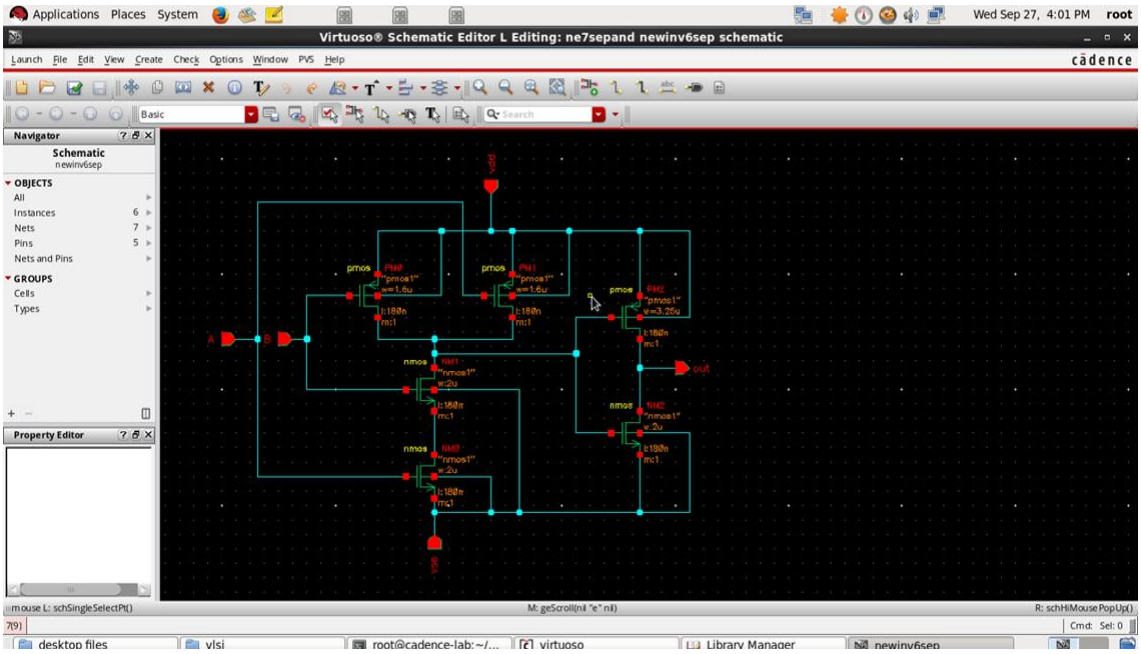

Fig.9.CMOSANDGateSchematics.

C.Adder

Itisabinarycircuitwhichisusedtoaddthreebitsandgivessumandcarryasoutputs.Wecanalsobuildfulladdercirc uit using twohalfadders.Incadencevirtuosotoolwebuiltadderusing28transistors.Aftercreatingsymbolweuseda testcircuittosimulatetheadderschematics.InQCAwiththe helpofclockingmechanism,wecreatedadderusing362cells.

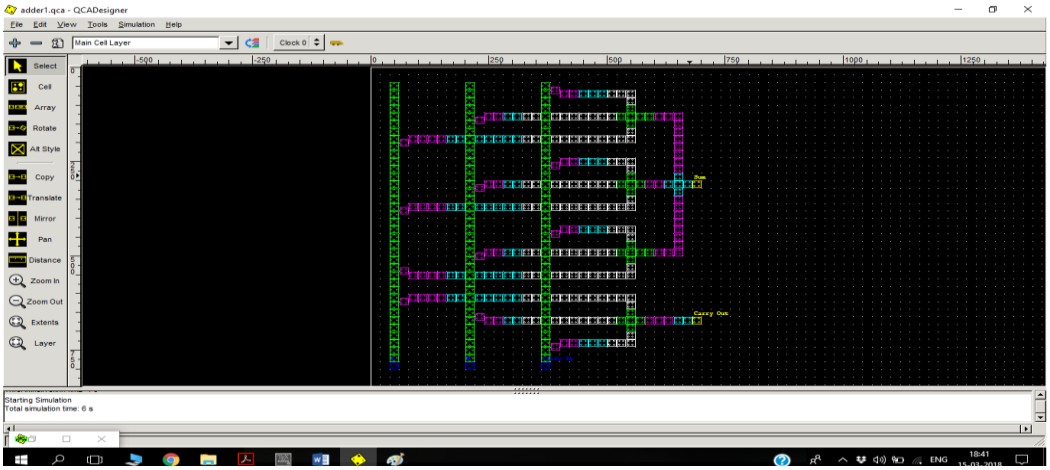

Fig.10.QCAAdderLayout.

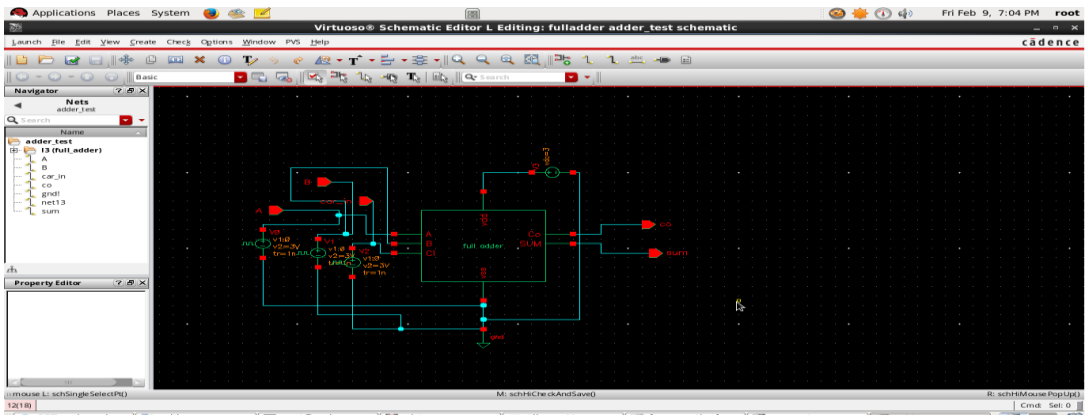

Fig.11.CMOSAdderSchematics.

D.1BitMemoryCell

ForCMOStechnologywareausing6TSRAMCell.Thestructureof6transistorSRAMcellsstores1bitofinformation.Thecellisformedbytwoinverterswhichareconnectedinbacktobackconfiguration.SRAMCellbasicallyworks withthehelpofWordLine(WL),Bitlines(BLand $\overline{BL}$)andAccesstransistors.Duringawriteoperation,theBitlinesworkasinputandwhenwewanttoreadfromthecellthebitlinesworkasoutput.ToturnoffthetheActivetransistorsmakethetheWordLineActiveLow.TowriteintothecelltheinformationisplacedonthebitlineandinverseinformationplacedonBL.TheAccesstransistorsareturnedonbymakingWordLineactivehighandtheinformationiswrittenintothecell.ThentheAccesstransistorsareturnedofftostoretheinformation.Duringreadoperationinformationisaccessedusingbitlinesbyturningonaccesstransistors.Wehavetocreatetwodifferentschematicsforreadandwriteoperations.Inordertoperformreadoperationweneedprecharagecircuitstochargetheprechargecapacitors.Wealsohavetoassumepredefinedconditionindicatingwhichbitisstoredthatis Bit0orBit1.InQCA,wecanusealoopbasedmemorycelltostore1bitofdata.HenceinQCAweneedonlyonecircuittostore 1bit.

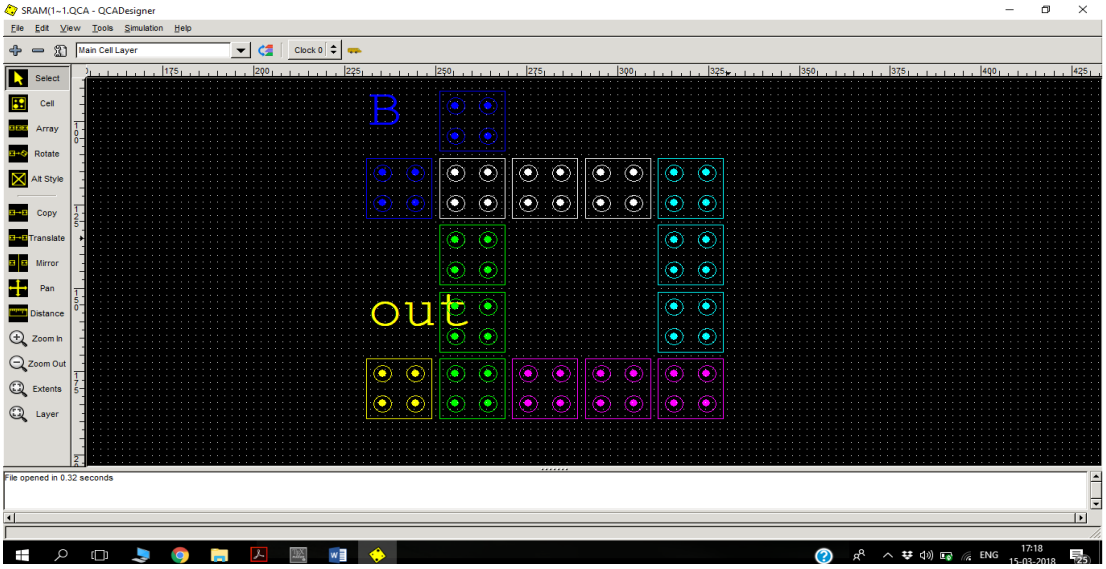

Fig.12.QCAMemoryCell.

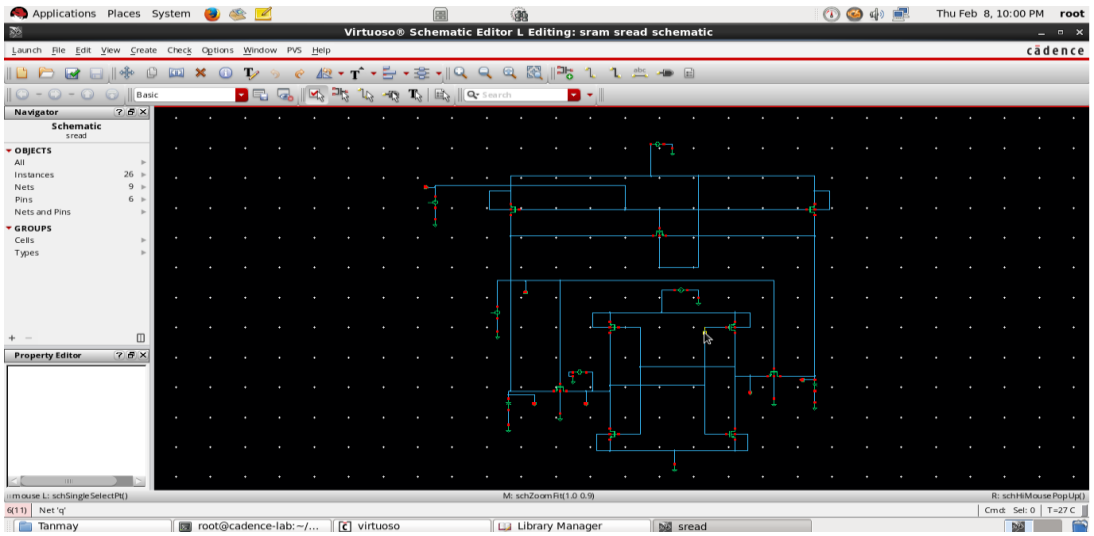

Fig.13.CMOS6TSRAMREADCircuit.

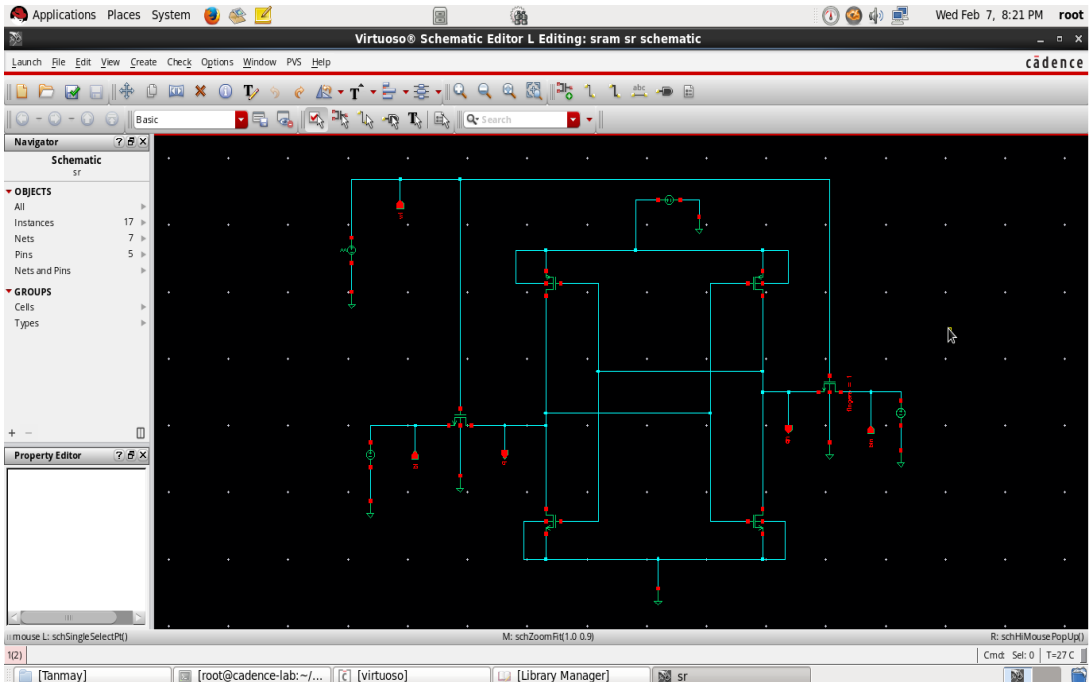

Fig.14.CMOS6TSRAMWRITECircuit.

III. SIMULATION RESULT

ThedesignandsimulationofInverter,ANDgate,Adderand1BitMemoryCellinCMOS,aswellasQCAtechnology, arepresentedinthispaper.Incomparisonwithotherstudies,thepresentedcircuitsinQCAactsasapipelinethatdecreasesdelaysandincreasesoperatingspeed.TheQCADesignerisusedtoconstructthelayoutandfollowinglayoutalsocanbesimulatedusingQCADesignersoftwaretool.TheQCAPROToolprovidesPowerDissipationandPolarizationintheformofGUI.CadenceVIRTUOSOToolisusedforsimulatingtheCMOSbasedschematicsandusingitsCalculatorfunctionwecanfindPowerDissipationandDelay.Theresultsshowedthattheproposed QCA based Circuits performs a task with reduced area and complexity in terms of a number of cells when compared to CMOS based Circuits.

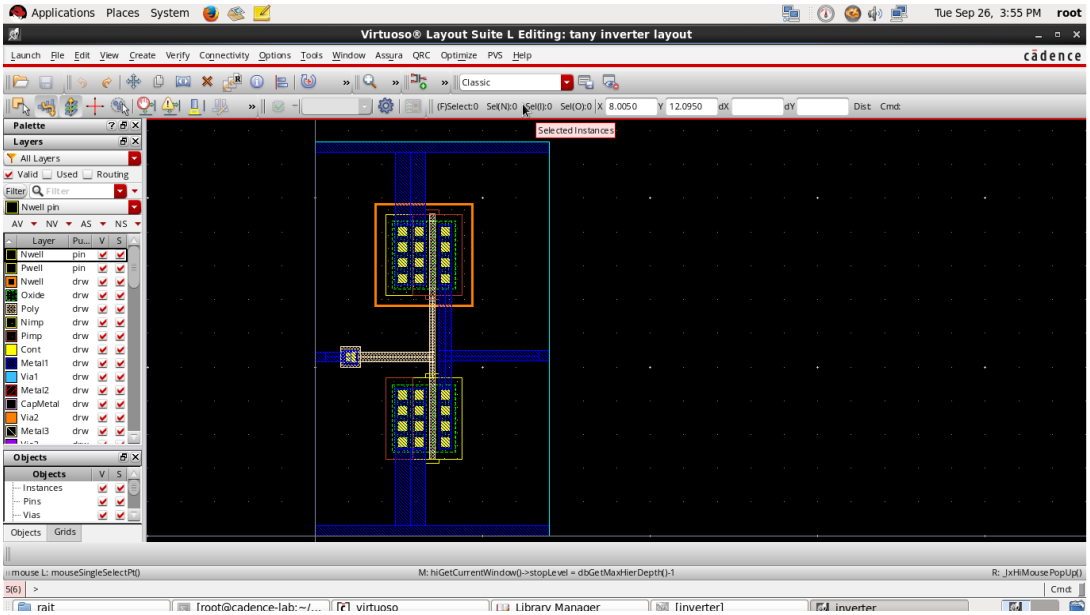

Fig.15.CMOSInverterLayout.

InverterLayoutisusedtoevaluatetheareaofthecircuit.
Areaoftheothercircuitsisalsocalculatedusingtheirrespectivelayouts.

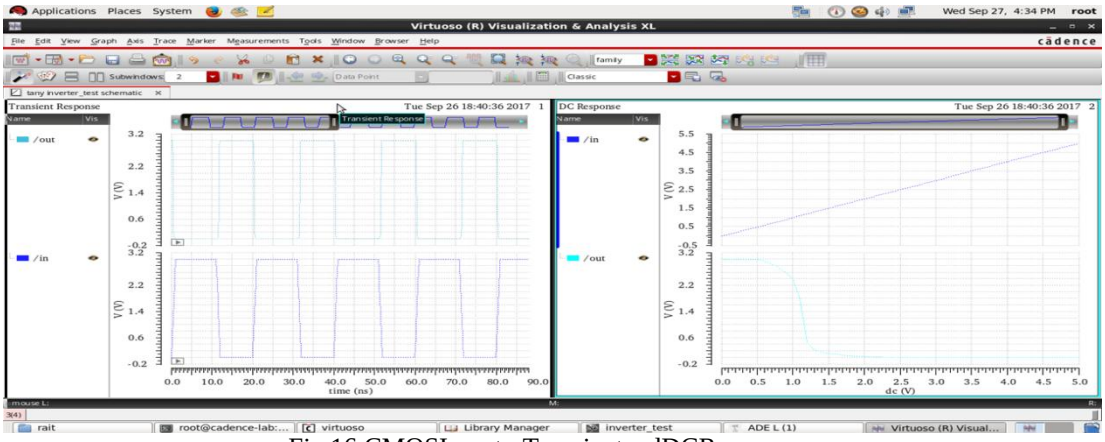

Fig.16.CMOSInverterTransientandDCResponse.

Usingthewaveformoftransientresponsewecanevaluatethe DelayandPowerDissipation.

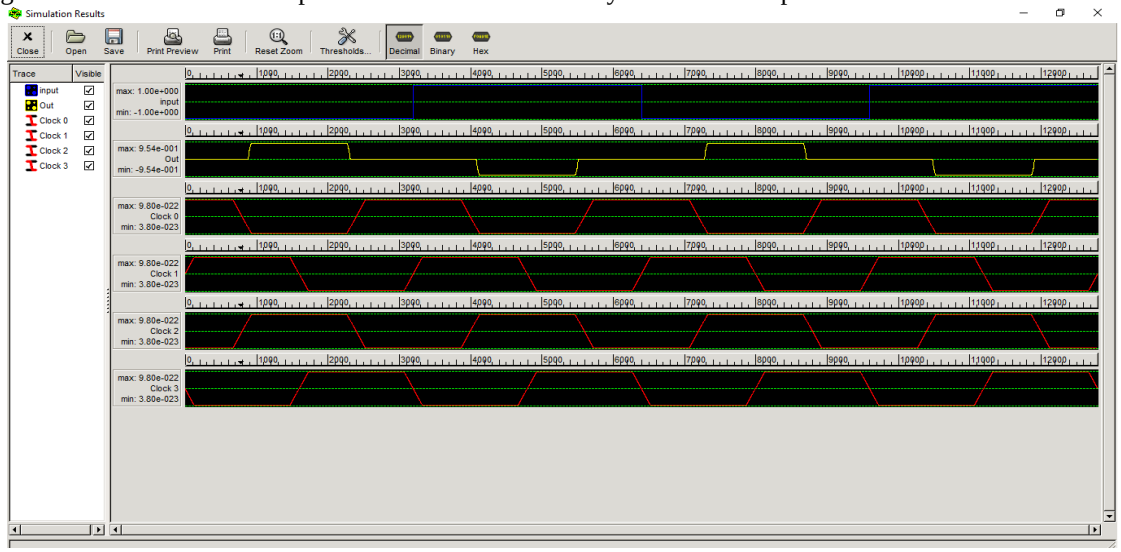

Fig.17.SimulationofInverterinQCA.

TheQCAPROToolrepresentsthePowerDissipationand PolarizationintheformofGraphicalUserInterface(GUI).

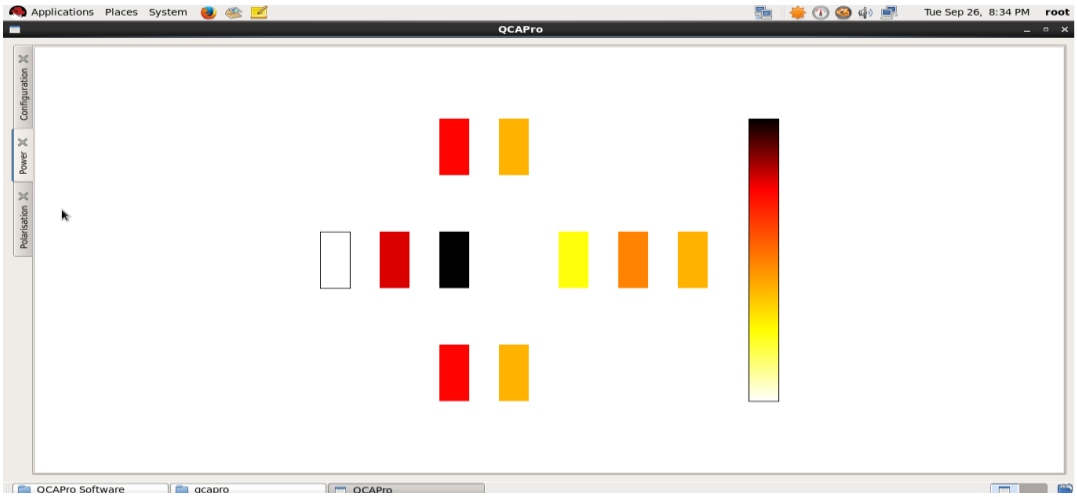

Fig.18.InverterPowerDissipationinQCA.

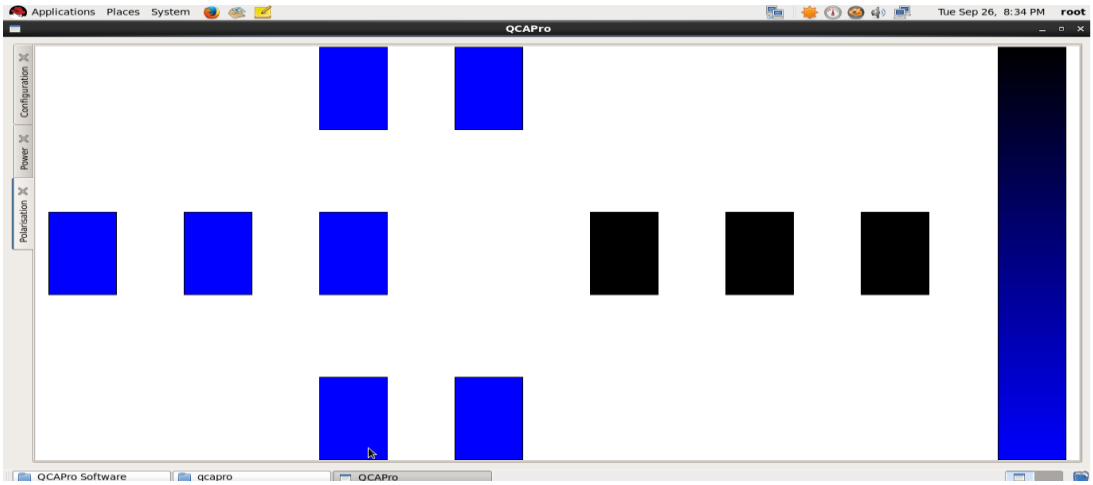

Fig.19.InverterPolarizationinQCA.

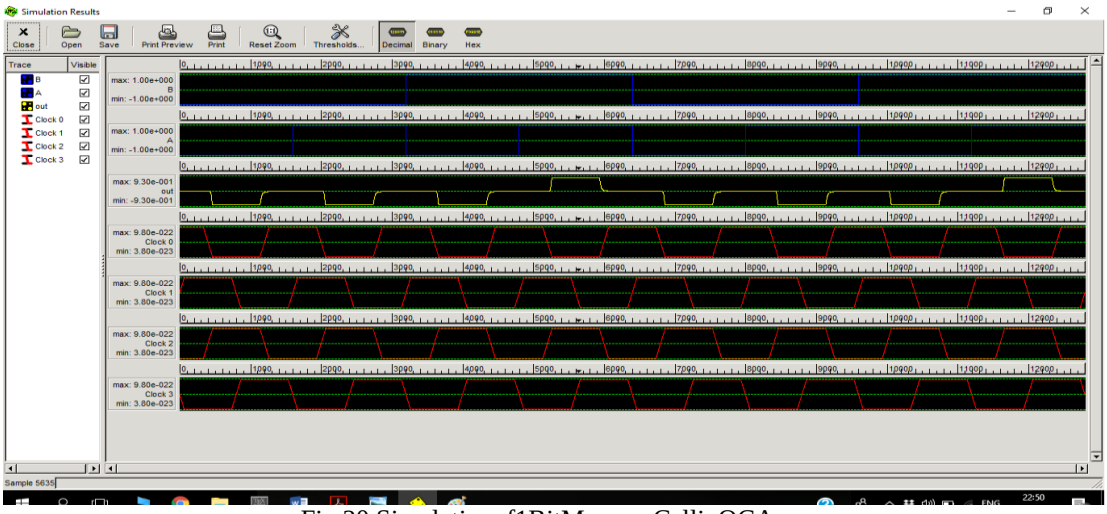

Fig.20.Simulationof1BitMemoryCellinQCA.

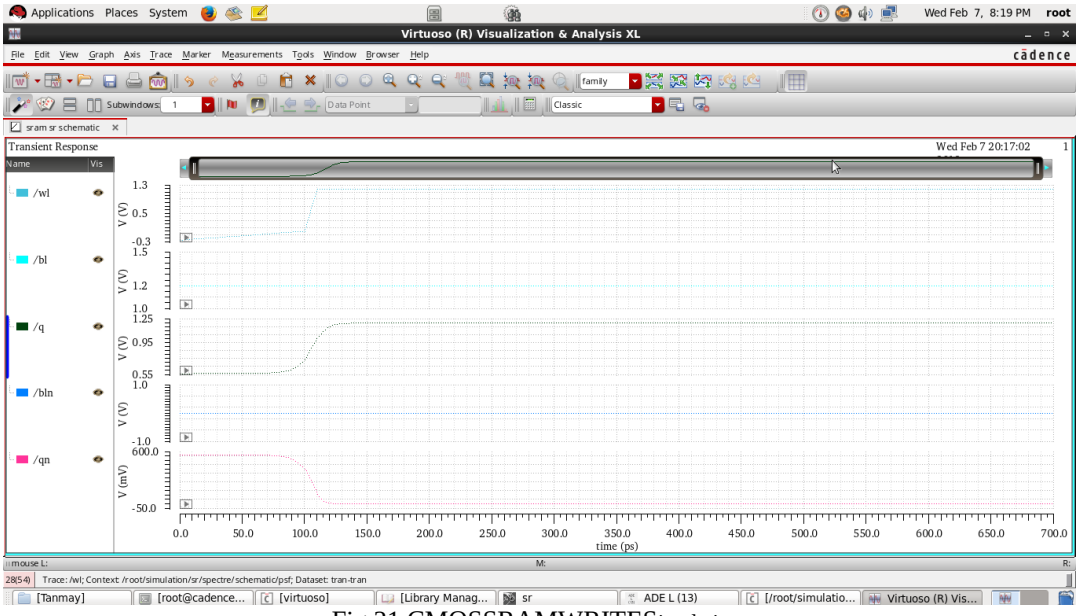

Fig.21.CMOSSRAMWRITESimulation.

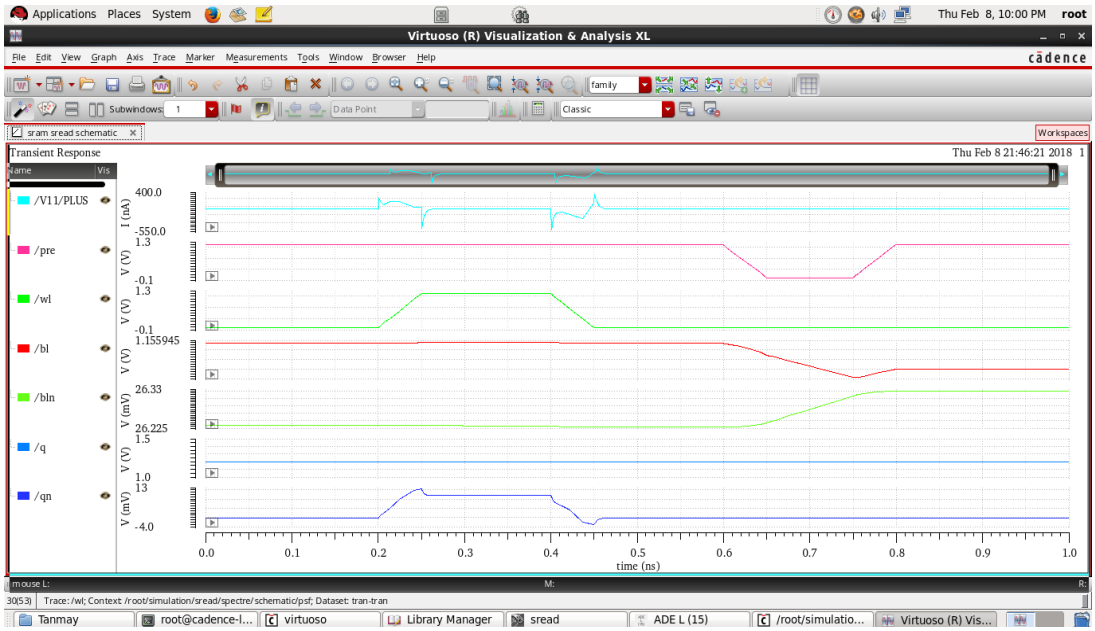

Fig.22.CMOSSRAMREADSimulation.

Sr No.	Component Circuit	CMOS				QCA			
		Area	Complexity	Delay	P.D.	Area	Complexity	Delay	P.D.
1	Inverter	68.11 um^2	2 T	507.0E-12	1.31 uW	6.804 um^2	10 Cells	-	GUI
2	AND	175.906 um^2	6 T	131.1E-3	1.639 uW	2.916 um^2	5 Cells	-	GUI
3	ADDER	1615.52 um^2	28 T	-73.6E-3	2.763 uW	406.296 um^2	362 Cells	-	GUI
4	1 Bit Memory Cell READ	223.35 um^2	8 T	-25.62E-12	1.156 uW	8.10 um^2	15 Cells	-	GUI
5	1 Bit Memory Cell WRITE	201.04 um^2	6 T	2.562E-3	1.2 uW				

ComparisonTable.

IV. CONCLUSION

TheresultsshowedthatthedifferentQCAbasedcircuitsperformsataskwithreducedareaandcomplexityinterm sof anumberofcellswhencomparedtoCMOSbasedcircuits.TABLEshowsthecomparisonbetweenQCAandCadence withdifferentparameterslikedelay,powerdissipation,polarization.Thusourproposedpaperhaveovercometheproblem s inCMOStechnologyonthenanoscale.Itisexpectedthatthis workwillgiveinsighttomanyfutureQCAarchitectures.

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Withthehumorousdelectation,Wemakeuseofthisop-portunitytoexpressourdeepsenseofthankfulnesstoour guide,Mrs.SushmaKodagaliforherincitement,motivationandforinvigoratingandrectifyingthevariousreportsofour swithawareness,andministration.Shehastakentheassistancetogoacrosstheprojectandmakeimperativealterationsw henrequired.Itassistedustoworkintheproperorientationandto achievethedesiredobjective.Wewouldliketothankour HeadofElectronicsDepartmentVishweshVyawahareandPrincipalDr.RameshVasappanavaraftheirbraceandinsp iration.Ouradmirationandthanksalsogotoourcollegeinthrivingtheprojectandtothepeoplewhohaveenthusiastically helpedus withtheircapabilities.

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