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Design of 4 Bit Alu Using Modified Gdi Technology for Power Reduction

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ABSTRACT*: In day to day development of transportable digital applications, the requirement for reducing delay, decreasing in size, and low power dissipation various analysis efforts . We would like to enhance the performance of logic circuits, once supported ancient CMOS technology, and resulted within the development of the many logic style techniques throughout the last twenty years. GDI (Gate diffusion input) is a method of low power digital combinable style. This method permits less power consumption and reduced propagation delay with minimum range of transistors as compare to alternative presently used logic style designs, like CMOS, PTL, CPL and TG. XOR was enforced victimization the accessible technologies & ascertained that GDI technology is giving less power consumption. But within the GDI technology output voltage swing degradation, fabrication complexness, & power consumption issues are the disadvantages. Attributable to this reason changed GDI was planned. Modified GDI technology is additional economical in terms of power consumption, fabrication complexness, and low output voltage swing degradation when put next to GDI technology. The ALU consists of 2×1MUX, 4×1MUX and full adder circuits. These circuits were implemented using Tanner EDA tools. The 4-bit ALU and its blocks were designed using GDI& modified GDI. Comparative study states that Modified GDI giving low power consumption. .*

KEYWORDS - *ALU, Gate Diffusion Input (GDI), Modified GDI, low power*

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I. INTRODUCTION

Market demand for mainly three things: low power, high speed and less area for designing the circuit. So intensified research is going on low power, high speed embedded systems used in mobiles, laptops etc has led to scale down technology to nano regimes, allow to implement more functionality on single chip. The power and area are the major problems in ALU implementation, so that we preferred low power logic design style i.e. GDI. This technique allows less power consumption and reduced propagation delay with minimum number of transistors as compare to other currently used logic design styles, like CMOS, PTL, CPL and TG. The ALU and its blocks were implemented using GDI technology. But in the GDI technology output voltage swing degradation, fabrication complexity & power consumption are the disadvantages. Due to this reason Modified GDI was proposed. The Modified gate diffusion input (MOD-GDI) technology is more efficient in terms of power consumption, fabrication complexity and low output voltage swing degradation when compared to GDI technology.

1.1Main Objective

The main objective of the project is to design a power efficient ALU by using Modified GDI technology. Traditional full adder, 2×1MUX &4×1MUXare replaced with Modified GDI technology.

Following are the main objectives:

1. Reducing the power consumed by existing ALU.
2.To maintain output voltage swing degradation considerably.
3. Reduce the fabrication complexity of the circuit.

II. Gdi (Gate Diffusion Input)

GDI is the technique of low power digital combinational circuit design. This method permits the reducing power consumption, delay, transistor count and space of digital circuits, whereas maintaining low complexness of logic style.

Table 1-: XOR design using different technologies

Technology	No. of Transistors	Area (in pico meters)	Delay (in µ sec)	Power (in µ watts)
CMOS	14	8.75	0.050702	22.69725
PTL	4	2.5	0.10001	0.06605722
TG	8	5	0.10001	0.5605967
CPL	6	3.75	0.10120	0.1834376
GDI	4	2.5	0.10009	0.0001057771
MODIFIED GDI	4	2.5	0.10023	0.000080777

The table 1 gives XOR design was enforced mistreatment totally different technologies. Finally we have a tendency to discover the GDI is a lot of benefits than all alternative technologies like CMOS, CPL, PTL and Transmission Gate. Modified GDI gives very less power than the GDI is clearly observed in table 1.

2.1 Advantages of GDI
The main advantages of GDI are

- Less power consumption
- Less area
- Required less number of transistors
- Efficient for placement & routing

- Shorter interconnects
- High speed operations(less delay)
- Less crosstalk.

2.2 Draw Backs of GDI
The drawbacks of GDI are

- Output Voltage swing degradation
- Power consumption
- Fabrication complexity.

III. MODIFIED GDI

The limitations of GDI can be overcome by modified gate diffusion input (Mod-GDI) logic style.
3.1 Advantages of Mod-GDI
3.1.1 Fabrication complexity

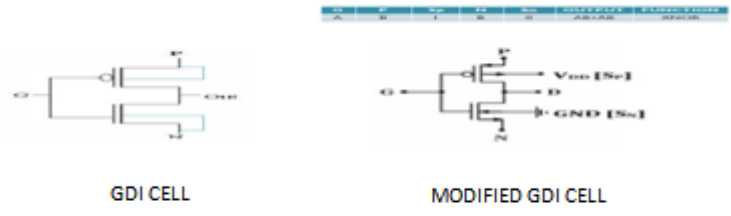


Figure (1): Basic cells of GDI and MOD-GDI

Figure 1 shows thebasic cell of GDI and Modified GDI. In GDI cell the body of the PMOS is connected to one of the input (P) & the body of NMOS is connected to another input of GDI (N). So that the body voltages of

PMOS as well as NMOS are varied according to the inputs of P & N. Due to this, the fabrication of the circuit is very complex. This problem is rectified in Modified GDI cell, the body of PMOS is connected to some DC supply voltage& the NMOS body is connected to ground terminal. Due to this the fabrication complexity of the circuit is reduced compared with GDI. The Modified GDI cell consists of five input terminals.

3.1.2 Output voltage swing degradation

Figure 2 shows the waveform of full adder implementation using GDI technology. Sum and Carry outputs does not reach to their full swing (0V and Vdd volts) completely. Hence output voltage swing degradation problem occurs

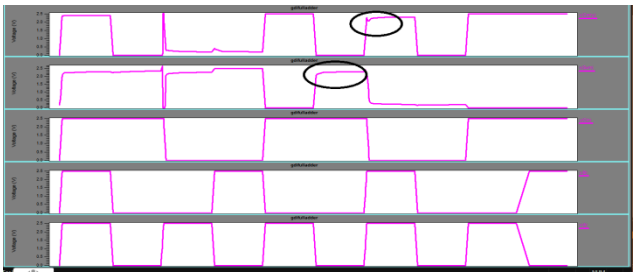


Figure (2) Simulated waveform of full adder implementation using GDI technology

Full adder was implemented using Modified GDI technology. The figure 3 shows the waveform of the full adder circuit using Modified GDI technology. The output voltage swings between 0 and Vdd volts and swing degradation problem is rectified in Modified GDI full adder design.

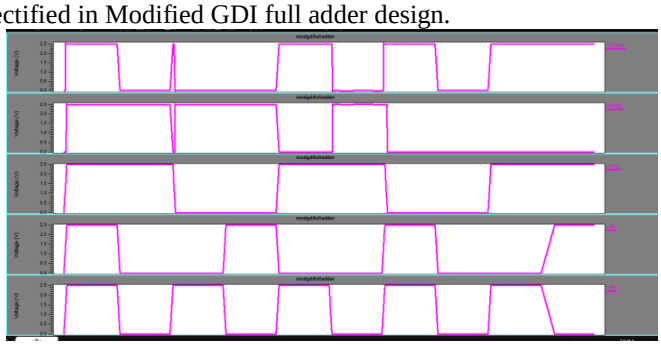
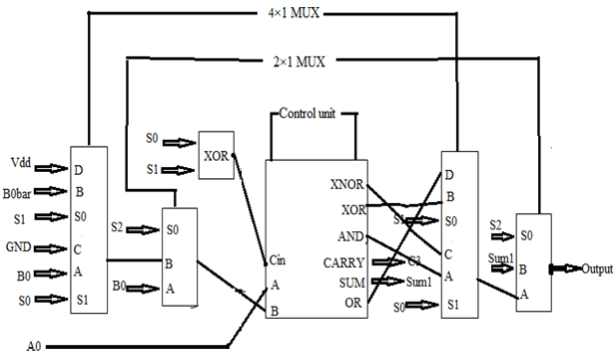


Figure (3) Simulated waveform of full adder implementation using MOD-GDI technology

IV. IMPLIMENTATION OF ALU

The ALU consists of two 2×1MUX, two 4×1MUX and one full adder circuits.

4.1 One-bit ALU:



V. Operation:

Figure (4) shows the block diagram of one-bit ALU. The first 4×1 MUX takes the four inputs – Vdd, GND, B0, B0bar and selection bits S0, S1. Depending on the selection bits the 4×1 MUX gives any one of the input as an

output. The first 2×1 MUX takes the one input from the first 4×1 MUX, second input as B0 & selection bit S2 then the output of 2×1 MUX is any one of the input based on selection bit. The processing unit consists of full adder, AND & OR logics.The processing unit having three inputs and produce six outputs. The inputs of processing unit are A0, output of XOR, output of first 2×1 MUX depending on these three inputs the processing unit performs the XOR, XNOR, AND, OR, Full adder operations. The second 4×1 MUX connected to the outputs of processing unit, depending on the selection bits S0, S1 the 4×1 MUX produce the output. The second 2×1 MUX takes the one input from the second 4×1 MUX, other input as Sum & selection bit taken as S2, based on the selection bit the 2×1 MUX gives the final output.

The four bit ALU was implemented using this one bit ALU circuit. Four one bit ALUs are needed for the designing of 4-bit ALU. The ALU performs the different operations based on the three selection bits S0, S1, S2. If the S2, S1, S0 values are varying from 000 to 111 then the ALU performs AND, XOR, XNOR, OR, ADD, SUB, INC, DEC operations with respectively. The table 2 gives the operations of ALU, based on status of the select signals.

Table 2-: Truth table of ALU

Selection lines			
S2	**S1**	**S0**	**OPERATIONS**
0	0	0	AND
0	0	1	XOR
0	1	0	XNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	INCREMENT
1	1	1	DECREMENT

First we design the ALU blocks - 4×1 MUX, 2×1 MUX & processing unit. After words we design the ALU. Figure (5) shows the ALU blocks implementation using GDI with 180nm technology. Full adder, AND, OR logics are combine to form processing unit.

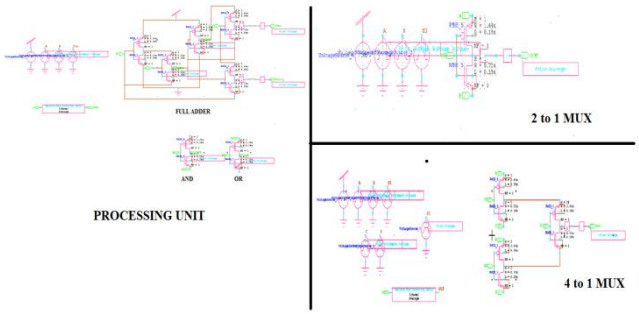


Figure (5) ALU blocks implementation using GDI

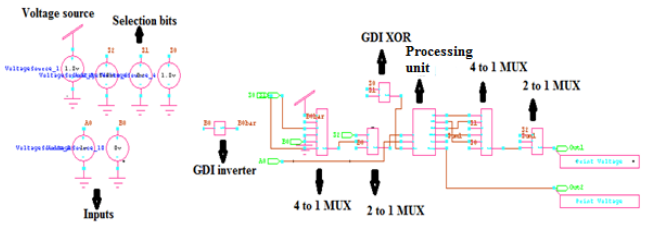


Figure (6) 1-bit ALU design using GDI

The figure (6) shows the 1-bit ALU design using GDI, the processing unit, 4×1 MUX, 2×1MUX rectangular boxes are symbols of those related circuits.

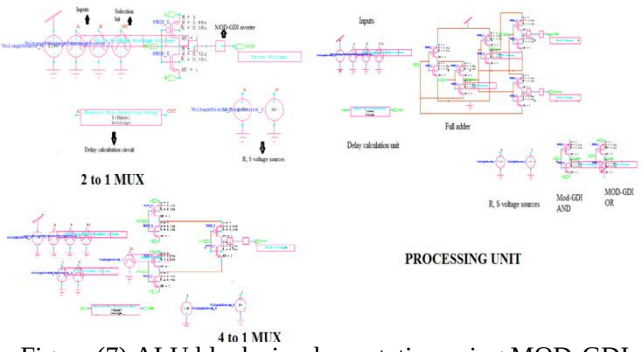


Figure (7) ALU blocks implementation using MOD-GDI

The figure (7) shows the implementation of ALU blocks using modified GDI. R, S are the voltage sources, 'R' is connected to the body of PMOS, 'S' is connected to the body of NMOS. This is the difference between the GDI & modified GDI.

4.2 Four-bit ALU:

4.2.1 4-bit ALU using GDI:

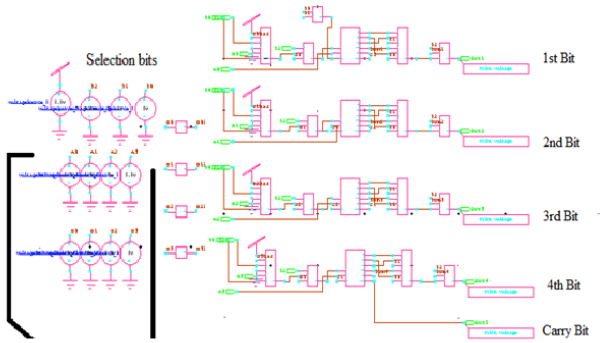


Figure (8) 4-bit ALU implementation using GDI

The figure (8) shows the 4-bit ALU design using GDI logic, 4-bit ALU consists of three selection bits, eight 4×1 MUX, eight 2×1 MUX & four processing units.

4.2.2 4-bit ALU using MOD-GDI:

Figure (9) shows the 4-bit ALU design using MOD-GDI logic, the rectangular boxes are symbols of circuits, in this design we are using four MOD- GDI inverters, one MOD-GDI based XOR gate.

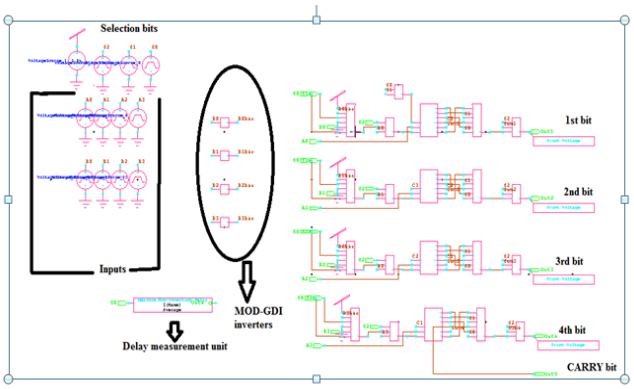


Figure (9) 4-bit ALU implementation using MOD-GDI

VI. RESULTS

The performance evaluation of existing GDI designs and the proposed MOD-GDI designs is carried out using Tanner tools in 180nm. All the parameters such as delay and total power dissipation are tabulated.

5.1 Functional verification of 1-bit ALU:

The 1-bit ALU SUBTRACTION function can be verified by applying S2, S1, S0 equals to 1, 0, 1 respectively. Let us consider A0 is a pulse signal, B0= 0, then we observe the function output of 1-bit ALU [A0-B0=OUT].

- The output is equals to logic one when A0 equals to logic one that means logic one- logic zero= logic one and the output is equals to logic zero when A0 equals to logic zero [logic zero-logic zero=logic zero].
- Carry of the 1-bit ALU depends on the processing unit inputs, in this selection [S2, S1, S0= 101] Carry equals to logic one.

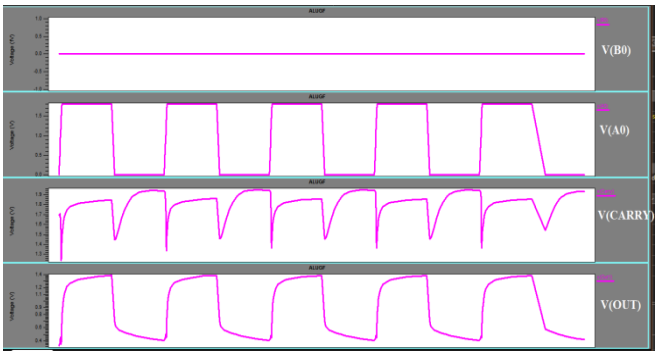


Figure (10) SUBTRACTION function of 1-bit ALU using GDI

Figure (10) shows the subtraction function of GDI based 1-bit ALU, the output of 1-bit ALU maintain logic one and logic zero regarding to the A0 value and the carry maintain logic one. The voltage swing of output wasdegraded in GDI based 1-bit ALU.

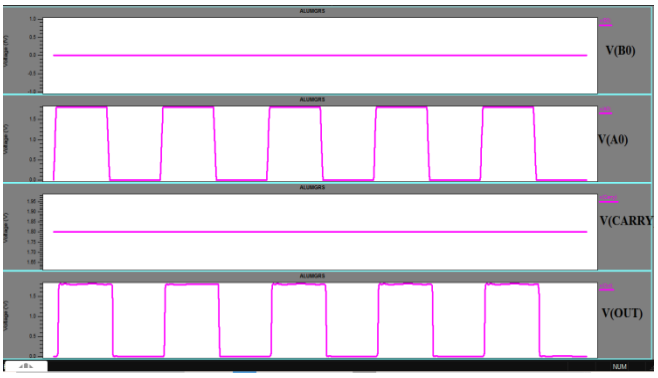


Figure (11) SUBTRACTION function of 1-bit ALU using MOD-GDI

The figure (11) shows the subtraction function of MOD-GDI based 1-bit ALU; the output voltage swing degradation problem in GDI was rectified in MOD-GDI.

5.2 Comparison between GDI and MOD-GDI in 180nm Technology

Table 3-:Comparison between GDI & MOD-GDI based on 2× 1 MUX

TECHNOLOGY	POWER CONSUMPTION In µ watts	DELAY In nano sec	POWER DELAY PRODUCT In atto
GDI	0.2140549	0.93306	199.726
MOD-GDI	0.09173824	1.4860	136.323

The table (3) gives the 2×1 MUX power consumption & delay using GDI and MOD-GDI. From the table MOD-GDI consumes less power than GDI but more delay in MOD-GDI.

Table 4-: Comparison between GDI & MOD-GDI based on 4× 1 MUX

TECHNOLOGY	POWER CONSUMPTION In nano watts	DELAY In pico sec	POWER DELAY PRODUCT In zepto
GDI	1.517131	3.2245	4.8920
MOD-GDI	0.03350261	3.9470	0.1322

The table (4) gives the comparison between GDI & MOD-GDI based on 4×1 MUX design; from the table, MOD-GDI gives less power consumption & better power delay product.

Table 5-:Comparison between GDI & MOD-GDI based on Full Adder

TECHNOLOGY	POWER CONSUMPTION In nano watts	DELAY In nano sec	POWER DELAY PRODUCT In femto
GDI	20.71192	50.667	1.04941
MOD-GDI	0.4483170	50.926	0.02283

Table (5) gives the full adder design using GDI & MOD-GDI and compare both in terms of power consumption & delay. From the table the MOD-GDI gives very less power consumption compared with GDI.

Table 6-:Comparison between GDI & MOD-GDI based on processing unit of ALU

TECHNOLOGY	POWER CONSUMPTION In nano watts	DELAY In nano sec	POWER DELAY PRODUCT In femto
GDI	22.81078	50.650	1.15537
MOD-GDI	0.4041265	51.007	0.02061

The table (6) gives the processing unit of ALU power consumption & delay values using GDI and MOD-GDI; it is the main block of ALU. From the table, the power & delay are optimized in MOD-GDI based processing unit.

Table 7-: Comparison between GDI & MOD-GDI based on 4-bit ALU

TECHNOLOGY	DYNAMIC POWER CONSUMPTION (when A=1011 & B=0100) in µ watts	STATIC POWER CONSUMPTION in µ watts	TOTAL POWER in µ watts	DELAY in nano sec	POWER & DELAY PRODUCT in femto
GDI	468.909194	15177.6300	1518231.909	53.582	81349902.1
MOD-GDI	462.302648	2182.4080	2644.7106	17.901	47342.9645

The table (7) gives the 4-bit ALU power consumption & delay calculation using GDI & MOD-GDI; from the table, the MOD- GDI gives very less power consumption than GDI. The power & delay product of MOD-GDI is also optimized compared with GDI.

VII. Conclusion

The 2×1 MUX, 4×1 MUX, full adder & processing unit were designed using both GDI and MOD-GDI in 180nm technology with Vdd=1.8v, & W/L ratio = 4. The table (7) shows that the MOD-GDI gives 85.6% less power consumption than GDI. The draw backs of GDI technology had over come in MOD-GDI technology and the implementation of 4-bit ALU is done using MOD-GDI technology gives less power consumption compared with GDI technology.

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